A Low-Distortion *K*-Band GaAs Power FET

TUN S. TAN, MEMBER, IEEE, KEN KOTZEBUE, MEMBER, IEEE, DAVID M. BRAUN, JIM CENTANNI, AND DAVE MCQUATE

Abstract—A *K*-band low-distortion GaAs power MESFET has been developed by incorporating a pulse-type channel doping profile using molecular beam epitaxial technology and a novel 0.3 μm T-shaped gate. The low-distortion FET's offer about 10 to 15 dBc improvement in second-harmonic distortion compared to devices fabricated on a uniformly doped active layer. Significantly larger power load-pull contours are obtained with the low-distortion devices, indicating the improved linearity of these devices. In an 8–20 GHz single-stage broad-band amplifier up to 10 dBc improvement in harmonic performance has been achieved using the low-distortion device. This low-distortion device exhibits very linear transconductance (G_m) as a function of the gate bias (V_g). A typical 750 μm gate width device is capable of 26 dBm of output power with 6 dB of gain, and power-added efficiency in excess of 35 percent when measured at 18 GHz. At 25 GHz the device is capable of 24 dBm of output power with 5 dB associated gain.

I. Introduction

THE DESIGN and application of high-performance broad-band GaAs FET power amplifiers places a severe demand on the harmonic and intermodulation distortion characteristics of FET's. Microwave power FET's are finding increasing usage in communications applications and in the design of test equipment requiring extremely linear performance. For a narrow-band amplifier only the close-in distortion products, such as the third-order intermodulation distortion, are of primary concern to the designer. However, in a broad-band amplifier with more than one octave bandwidth the second-harmonic distortion is also of significant concern to the circuit designer.

The intermodulation–distortion characteristics of GaAs FET's and their relationship to device parameters and doping profiles have been studied and reported by various workers [1]–[5]. In this paper, we deal mainly with the second-harmonic distortion characteristics of the GaAs FET and its relationship to device parameters and doping profiles. Two important device nonlinearities, namely transconductance (G_m) and drain conductance (G_d), were analyzed and measured under various bias conditions. Their relative contributions to the harmonic distortion were analyzed by comparing the G_m and G_d nonlinearity of standard GaAs FET's with the low-distortion FET's.

The design, fabrication, and performance of low-distortion GaAs power FET's designed for operation up to *K*-band will be described. The design and fabrication of an 8–20 GHz broad-band amplifier using both standard and low-distortion devices will be presented, and the performance of these amplifiers will be compared.

Manuscript received August 24, 1987; revised December 22, 1987.

The authors are with the Microwave Technology Division, Hewlett-Packard Company, 1412 Fountaingrove Parkway, Santa Rosa, CA 95401.

IEEE Log Number 8820439.

II. Second-Harmonic Distortion and Doping Profile

Theoretical analysis [1]–[4] has shown that the dominant contributors to the distortion in GaAs FET's are the variation in the transconductance G_m with the gate voltage (V_g), and the variation in drain conductance G_d with the drain voltage (V_d). The following equations relate these device characteristics with the second-harmonic distortion of the device (see the Appendix for derivation).

For G_m nonlinearity only,

$$\text{second-harmonic/fundamental} = G_{m1}v_g/2G_{m0} \quad (1)$$

where $G_{m1} = dG_m/dV_g$.

For G_d nonlinearity only (i.e., $G_{m1} = 0$),

$$\text{second-harmonic/fundamental} = \frac{G_{d1}G_{m0}v_g}{2(G_{d0}+G_L)^2} \quad (2)$$

where $G_{d1} = dG_d/dV_d$.

The ratio of the second harmonic to fundamental as given by (1) depends upon the input signal level (v_g) and the ratio G_{m1}/G_{m0}, where G_{m0} is the transconductance at quiescent bias point. Similarly, from (2) the second harmonic is also dependent on the derivative of the output conductance. Both nonlinearities contribute to the total harmonic distortion of a FET.

It has been shown that tailoring of the doping profile is a powerful technique for achieving G_m linearity [6]. The relationship between the derivative of the transconductance G_{m1} and the channel doping profile of a FET is expressed in the following relationship:

$$G_{m1} = \frac{dG_m}{dV_g} = \frac{\epsilon_S^2 Z V_s}{qNX_d^3} \quad (3)$$

where N is the doping concentration, X_d is the gate depletion depth, V_s is the electron velocity, ϵ_S is the permittivity of GaAs, Z is the total gate width, and q is the electron charge. For minimum G_{m1}, i.e., constant G_m, X_d should be maximized.

0018-9480/88/0600-1023$01.00

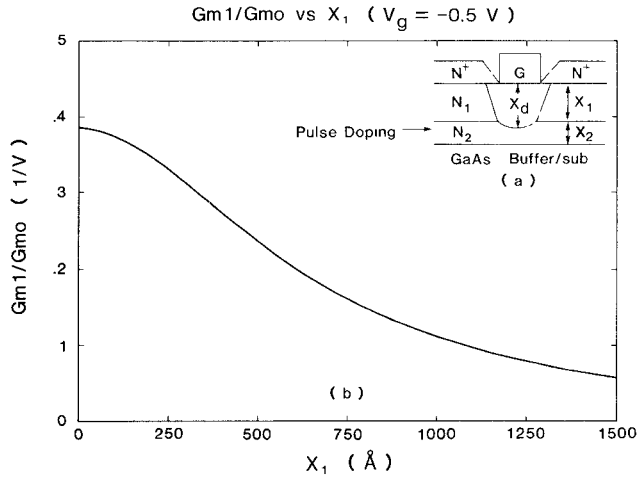


Fig. 1. G_{m1}/G_{m0} ratio versus thickness (X_1) of the low-doped layer ($N_1 = 3\times10^{16}$ cm^{-3}, $N_2 = 5\times10^{17}$ cm^{-3}, $\epsilon_S = 13.1\epsilon_0$, $\phi_t = 0.85$ V).

A design of the channel doping structure that can maximize the depletion width under the gate is shown in Fig. 1(a). The expression for the depletion width (X_d) for such a structure can be derived from Poisson's equation. Taking the electric field at the depletion edge to be zero and continuous across the N_1 and N_2 interface (Fig. 1(a)), the potential can be solved individually for each layer through integration and then combined. The result can be rearranged to give X_d:

$$X_d = \left[2\epsilon_S/qN_2(\phi_t - V_g) + (1 - N_1/N_2)X_1^2\right]^{1/2} \quad (4)$$

where ϕ_t is the built-in potential.

Equation (4) indicates that to maximize X_d we need to make $N_1 \ll N_2$ and the thickness (X_1) of the N_1 layer large.

By having the gate metal located in a low-doped region (N_1), the zero-bias depletion region can be extended slightly beyond the interface of the low-doped N_1 layer and high-doped N_2 layer, thereby making the X_d larger than the thickness of the low-doped N_1 layer. The product of thickness and doping of the high-doped (N_2) layer is predetermined by the desired current density of the device. Using (3), (4), and the expression for G_m [6], the ratio G_{m1}/G_{m0} (which is proportional to the ratio of second-harmonic output to fundamental output) is plotted versus the thickness (X_1) of the low-doped N_1 layer as shown in Fig. 1(b), indicating that low values of G_{m1}/G_{m0} can be reached with an (X_1) thickness of 1000 Å or more. This improvement in G_m linearity can result in an improvement in second-harmonic distortion by as much as 10 to 12 dB over a uniformly doped device as calculated by (1).

In order to fully realize the harmonic improvement due to the improvement in G_m linearity, it is important also to keep the harmonic distortion due to G_d nonlinearity small. The parameter G_d and its variation with drain voltage are among the least understood and controllable device parameters. They are affected by several parameters, including gate length, channel thickness, substrate resistivity, and substrate–channel interface effects [6]–[8]. To minimize the effect of substrate defects on G_d, a superlattice layer which consists of alternating layers of undoped AlGaAs and GaAs is incorporated as a buffer between the active channel and the substrate. The other important parameter which can affect G_d is the conductivity between source and drain of the channel as determined by the active channel thickness and its doping including the surface N$^+$ layer that is used to lower the parasitic resistances. Equation (2) indicates that to lower the harmonic contribution from G_d nonlinearity we need to minimize G_{d1} and maximize G_{d0}. The effect of the surface N$^+$ layer on G_d and G_{d1} was simulated using PISCES-IIB, a two-dimensional numerical modeling program [9]–[11].

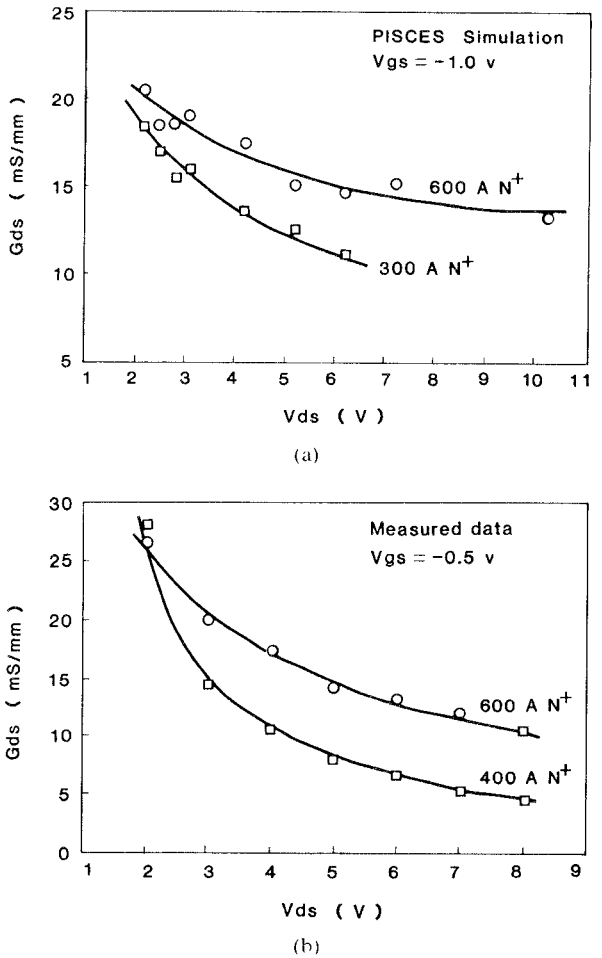


Fig. 2. Drain conductance (G_d) versus drain voltage for different surface N$^+$ thicknesses. (a) Simulated results with PISCES. (b) Experimental measured results. Surface N$^+$ doping is 1×10^{18} cm^{-3} in all cases.

Fig. 2(a) is a plot of output conductance G_d versus drain bias for surface N$^+$ thicknesses of 600 Å and 300 Å as calculated by PISCES-IIB. Fig. 2(b) is a plot of measured G_d versus V_d, which is obtained by first measuring small-signal S parameters of devices with different N$^+$ thicknesses at various drain voltages. G_d was obtained from the real part of the device output admittance Y_{22} measured at 575 MHz. As Fig. 2 illustrates, measurements of G_d versus V_d on devices with different surface N$^+$ thicknesses show the same trend and shape as seen with the simulated results. It can be seen that the device with 600 Å N$^+$

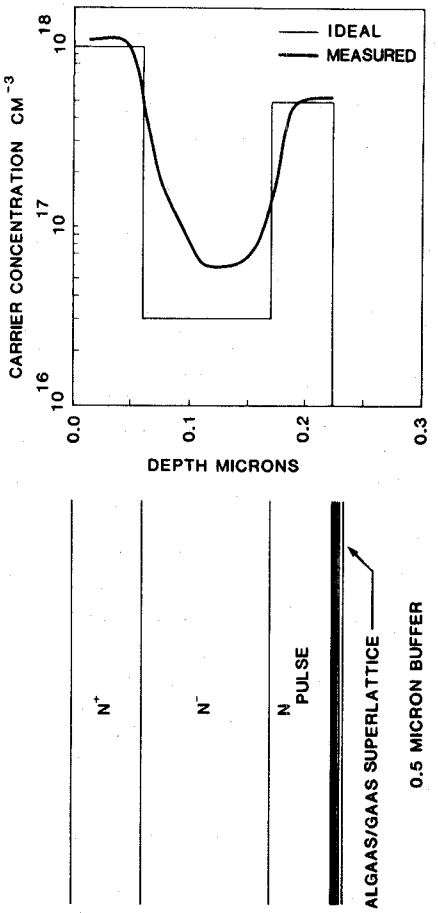


Fig. 3. Doping profile for low-distortion FET.

surface layer has smaller average slope (G_{d1}) and larger G_d than those of 300 Å or 400 Å N^+ surface layer devices. However, the conductivity of the channel or the thickness of the N^+ layer also has a strong effect on the gate-to-drain breakdown voltage [12]. An N^+ thickness of 600 Å was chosen in order to get a breakdown voltage greater than 12 V while minimizing the nonlinearity due to G_d. The resulting design of the device doping profile is shown in Fig. 3.

It can be shown that dC_g/dV_g, the derivative of gate capacitance, has the same dependence on depletion width (X_d) as G_{m1}. Even though our simplified analysis of harmonic distortion does not include C_g nonlinearity as a source for distortion, improvement in C_g nonlinearity via the doping profile for G_m linearity can also result in a further improvement in harmonic distortion.

III. Device Fabrication

Top and cross-sectional views of the low-distortion *K*-band GaAs FET are shown in Fig. 4. The device consists of two cells, each having ten 75 μm wide gate fingers which are combined by source air bridges to form a 750 μm wide cell. A Varian Gen II molecular beam epitaxial system was used to grow the different epi layers shown in Fig. 4. A superlattice buffer which consists of alternating layers of undoped GaAs and AlGaAs material is incorporated between the active layer and the substrate to improve the interfacial quality of the active layer and the substrate

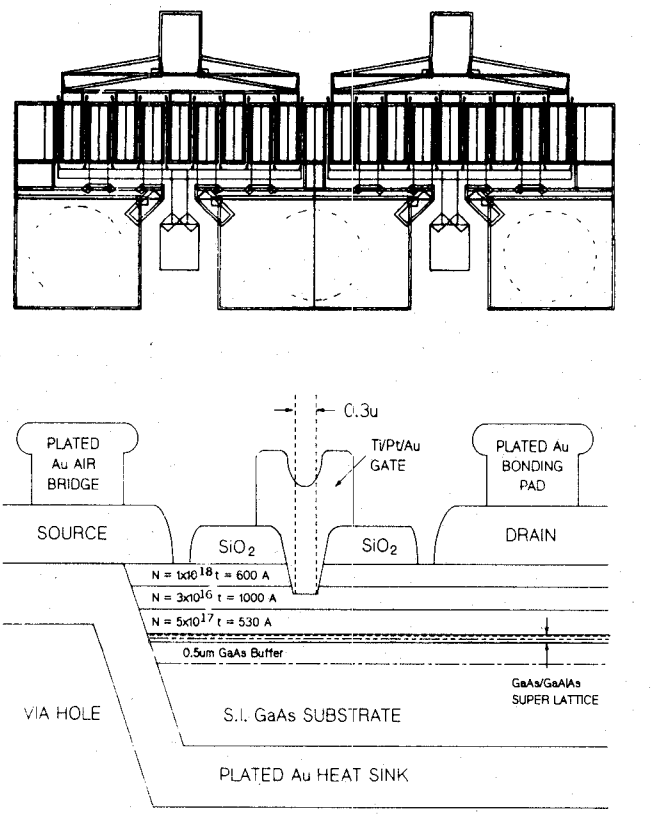


Fig. 4. Top and cross-sectional views of the *K*-band low-distortion GaAs FET.

[13]. During the MBE growth, two silicon sources are employed as N-type dopants for the active layers to ensure the sharp interface between the high-doped layers and the low-doped layer. The resulting doping profile is measured and shown in Fig. 3. The ability of MBE to reproduce closely the desired profile is excellent. After the epitaxial growth, a layer of CVD SiO_2 film was deposited on the wafer. The ohmic contact (NiCr, Ge, Au) was formed by a photoresist lift-off technique after the SiO_2 was chemically removed in the contact regions. The devices were isolated using H^+ ion implantation. Gate lengths of 0.3 μm were achieved using optical photolithography by evaporating aluminum at an angle into a 1.0 μm wide opening in the photoresist. The photoresist sidewall obstructs the coverage of the evaporated aluminum, resulting in a 0.3 μm opening of exposed SiO_2. The Al acts as a mask during the subsequent reactive ion etching of the exposed SiO_2. The Al and photoresist were then removed and a 1.0 μm gate opening again patterned into a new photoresist film. The 1.0 μm opening is centered about the 0.3 μm line etched into the SiO_2. Subsequent gate processing involves the formation of a gate trough by etching GaAs material in the 0.3 μm exposed region and the formation of the gate by photoresist lift-off of the deposited Ti/Pt/Au metal. The result is a unique, SiO_2 self-passivated, 0.3 μm T-shaped gate structure shown in Fig. 4 [14]. The typical gate metal resistance is 0.04 Ω/μm. The finished gates were protected from surface damage with 3000 Å of SiO. The smaller interdigitated source pads were connected to three large source pads through the use of Au-plated air bridges

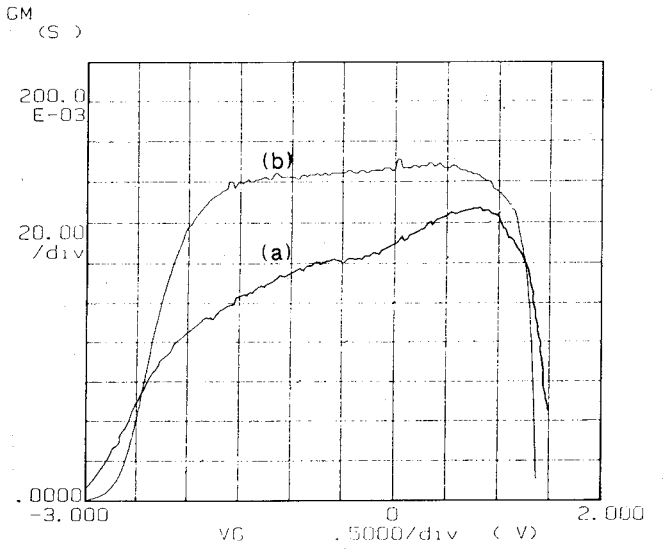


Fig. 5. G_m versus V_g scan for (a) standard uniformly doped device and (b) low-distortion pulse-doped device.

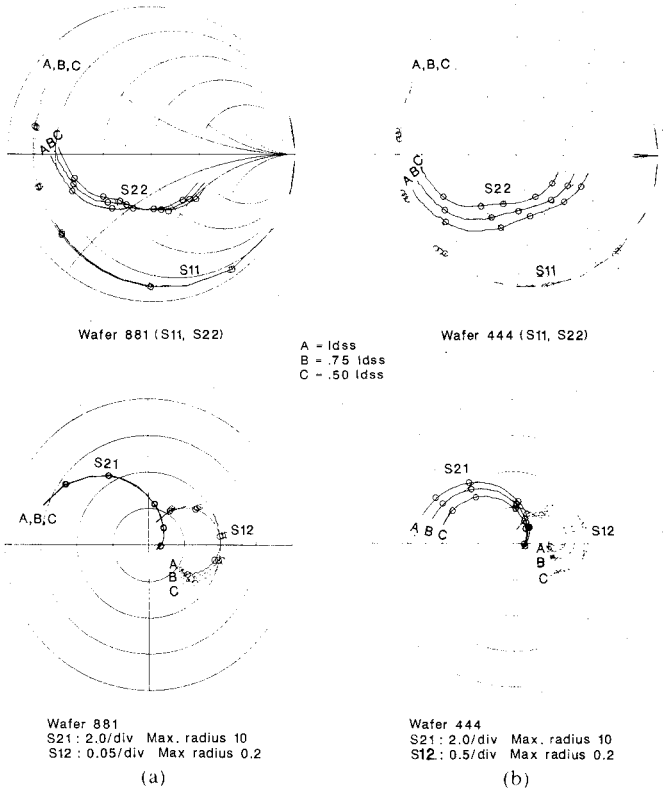
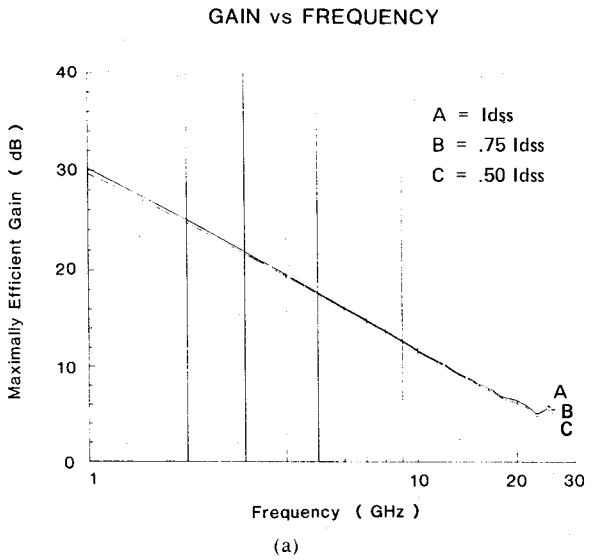


Fig. 6. S-parameter measurement from 0.5 to 26.5 GHz for (a) low-distortion and (b) standard uniformly doped device. (With $V_{ds} = 6$ V and $I_{ds} = 50$ percent, 75 percent, 100 percent of I_{dss} bias conditions. Markers indicate 1,2,5,10,20 GHz respectively.)

spanning across the gate feed. The air bridges were fabricated using a double photoresist procedure. The wafer was then lapped to a thickness of 70 μm and source contact was made by chemically etching via holes from the back of the wafer and plating gold to a thickness of 20 μm. The thick backside metal serves as a low-inductance common source connection and thermal heat sink for the device. The thermal resistance for the 1500 μm device was 25°C/W as measured using liquid-crystal techniques.



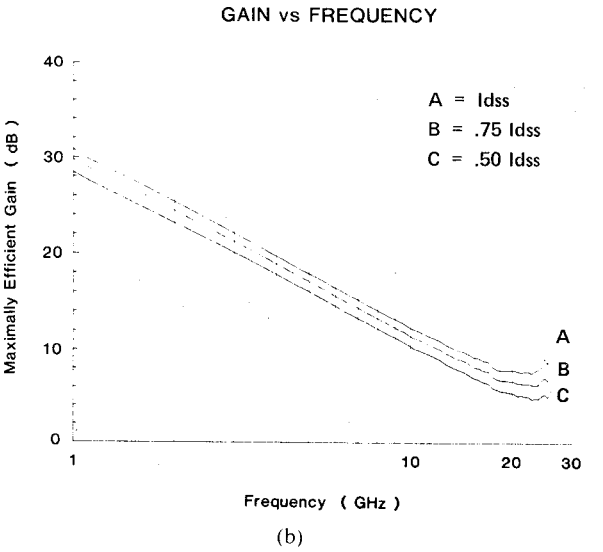


Fig. 7. Maximally efficient gain versus frequency for (a) low-distortion and (b) uniformly doped device (with $V_{ds} = 6$ V and $I_{ds} = 50$ percent, 75 percent, and 100 percent of I_{dss} bias conditions).

IV. Device Characteristics

Typical dc G_m versus V_g characteristics of the low-distortion FET and the standard FET fabricated on a 2×10^{17} cm^{-3} uniformly doped epi structure are shown in Fig. 5. The pulse-doped low-distortion device shows significantly more constant G_m versus V_{gs} than the standard uniformly doped device. Microwave characteristics of the devices were measured by bonding each device on a 50 Ω coplanar alumina substrate. S parameters of the devices were measured with an HP8510 Network Analyzer up to 26.5 GHz. Fig. 6 shows the measured S parameters under different gate biases. The pulse-doped device shows significantly smaller variation in S parameters versus gate bias than the uniformly doped device. The insensitivity of the S parameters to the gate bias is an indication of linearity of the device at microwave frequencies. Device maximally efficient gain [15] versus frequency calculated from measured S parameters for both types of devices is plotted in Fig. 7,

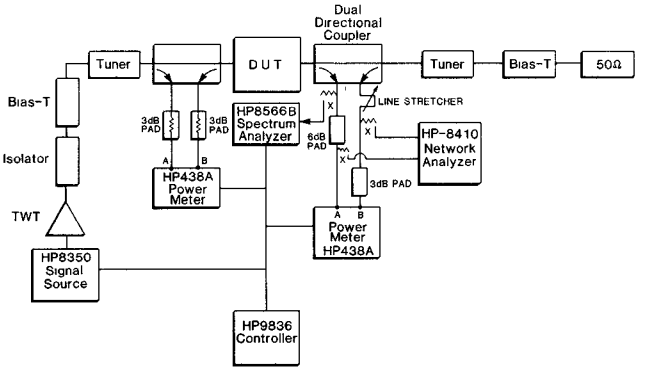


Fig. 8. 2–18 GHz load-pull system for measuring large-signal device and amplifier characteristics.

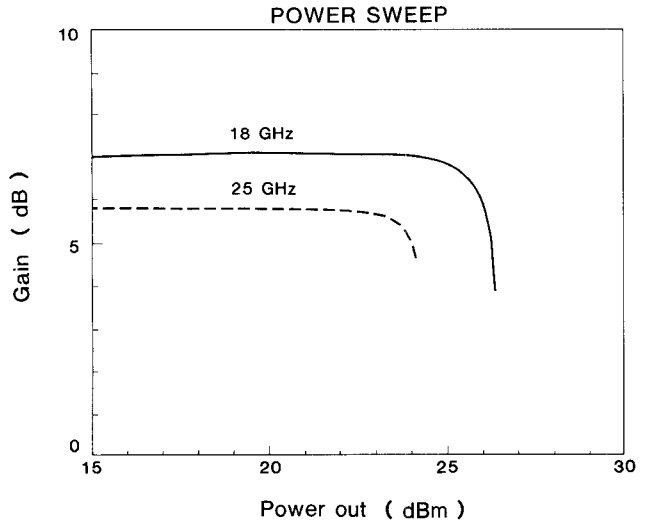


Fig. 9. Measured output power versus gain characteristics on pulse-doped FET at 18 GHz and 25 GHz (gate width = 750 μm).

showing usable gain up to 26 GHz. The gain of the pulse-doped devices shows significantly less variation with gate bias than the uniformly doped device.

Large-signal device characteristics up to 25 GHz were measured using a 2–18 GHz load-pull system (Fig. 8) and an 18–26 GHz waveguide load-pull system with active-load tuning [16]. Typical measured device gain versus output power for 18 GHz and 25 GHz is shown in Fig. 9. The gain and output power characteristics were very similar. Presented in Fig. 10 are the power and efficiency of the pulsed-doped device at 18 GHz. One dB gain compression output power is 26 dBm with 6 dB gain and power-added efficiency of 35 percent for a 750 μm wide cell. Load-pull contours were also measured for both pulse-doped and uniformly doped types of FET's. A typical set of data comparing the two types is shown in Fig. 11. The pulse-doped FET had larger contours than the uniformly doped FET; this desirable characteristic is believed to be a direct result of the improved linearity achieved with the pulsed-doped device. The harmonic distortion of the device was characterized using the HP8566B spectrum analyzer system shown in Fig. 8. The second-harmonic distortion was measured at various input power levels and output load conditions. Shown in Fig. 12 is a plot of second- and

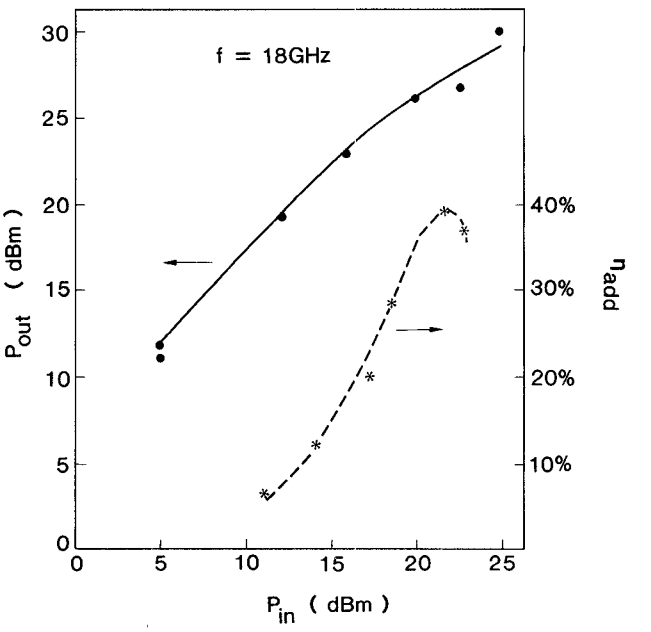


Fig. 10. Power and power-added efficiency versus input power of the 750 μm low-distortion FET.

third-harmonic distortion versus power at 3.5 GHz for uniformly doped and pulse-doped devices. Up to 10 dBc reduction in harmonic distortion is achieved using pulse-doped devices. Measurements at other frequencies yielded similar results. It is believed that this improvement is in large part the result of the improvement in G_m linearity and the results correlate well with the improvement predicted by (1).

V. Amplifier Design and Results

A single-stage 8 to 20 GHz amplifier was designed and constructed in order to evaluate and compare the large-signal performance characteristics of the uniformly doped and pulse-doped FET's. The design approach was to 1) experimentally measure the output loads which optimized output power as a function of frequency, 2) use this information to design a broad-band output load, and then 3) use the measured small-signal S parameters in conjunction with this output load to design an input matching circuit which optimized transducer gain over the 8 to 20 GHz design range.

The large-signal output load information was obtained from the 2 to 18 GHz load-pull system. Shown in Fig. 13 is a typical set of output load data for a uniformly doped FET, together with the model which was fit to the data. This model yields a best-fit approximation to the complex conjugate of the measured large-signal reflection coefficients, and has been found useful for purposes of computer-aided design. Measurements of the pulse-doped FET yielded similar results, so only one output circuit design was required.

Using the large-signal conjugate output load model of Fig. 13, an output circuit was designed to achieve a good "power match" over the 8 to 20 GHz frequency range. With a simple high-pass topology it was possible to ap-

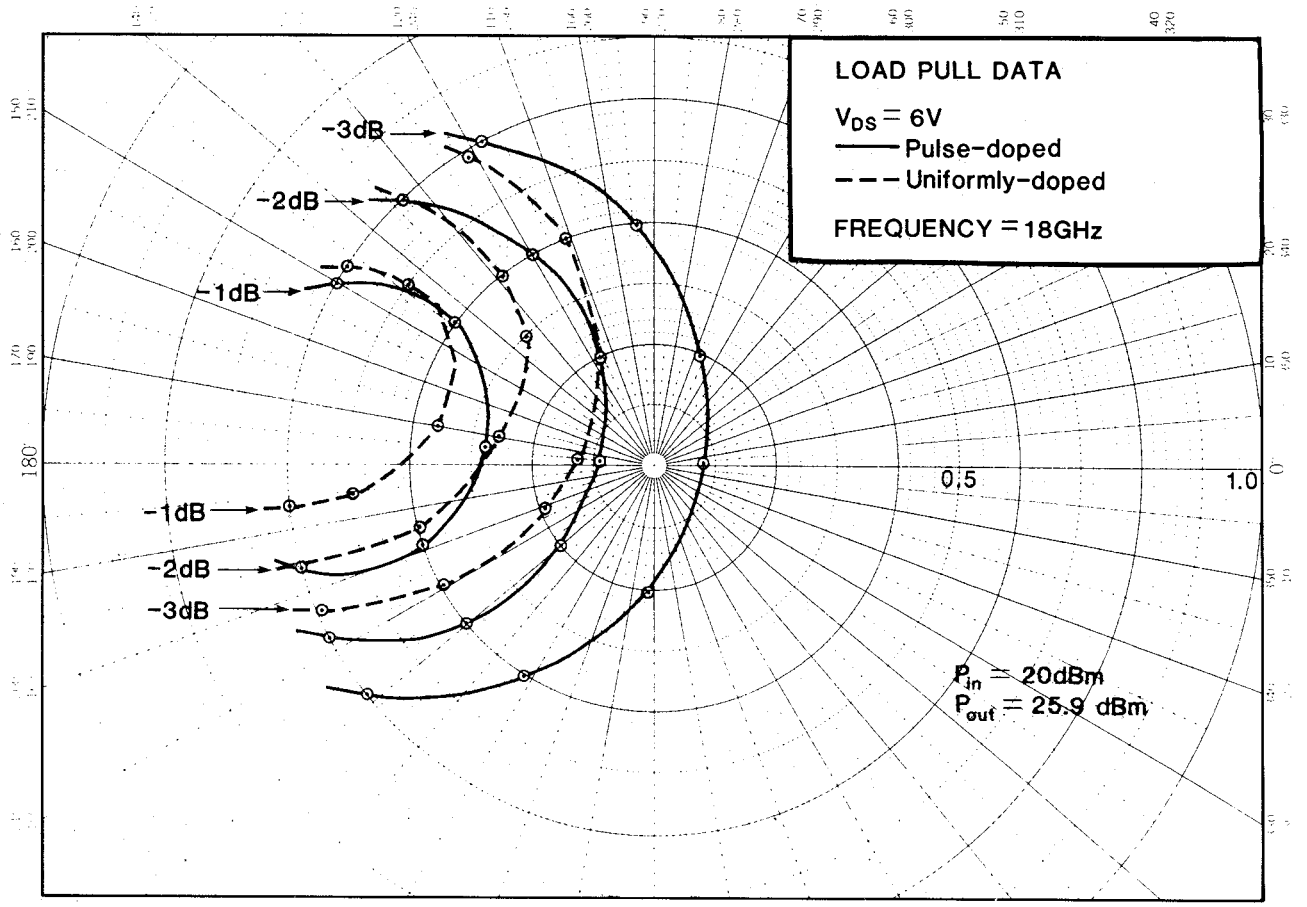


Fig. 11. Load-pull contours of the uniformly doped and pulse-doped devices.

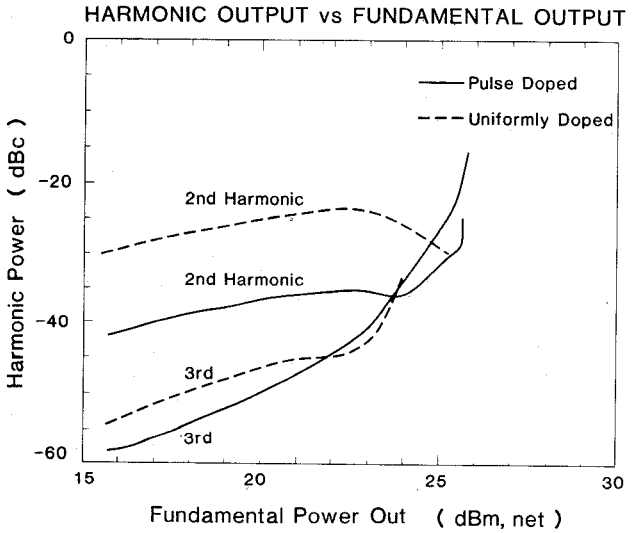


Fig. 12. Second- and third-harmonic distortion of the pulse-doped and uniformly doped devices.

proximate the optimum output large-signal load with a mismatch error of less than 0.5 dB over this frequency range. Small-signal S parameters were then used to design the input matching network, which utilized a low-pass topology. A schematic diagram of the resulting amplifier is shown in Fig. 14. This design was implemented in microstrip, using 0.005 inch thick sapphire substrates. Shown in Fig. 15 are the experimentally measured small-signal gains of both the uniformly doped and pulse-doped FET amplifiers. These results are in good agreement with computer simulations, with the measured gain at 20 GHz approximately 1 dB below the calculated gain, which is reasonable since no provision for circuit dissipation loss was included in the simulation.

The output power capabilities of the two amplifiers were also similar, with saturated output power of 25 to 26 dBm over the 8 to 20 GHz frequency range. The major difference between the two amplifiers, as expected, was in the level of second-harmonic distortion. Shown in Fig. 16 is a comparison of the measured second-harmonic distortion for the two amplifiers as a function of frequency at 20 dBm power output. The pulse-doped FET amplifier had second-harmonic distortion lower than the uniformly doped FET amplifier by about 10 dB over the 8–20 GHz frequency band.

The significant improvement in second-harmonic distortion obtained with the pulse-doped FET is useful only if the distortion products arising from higher order nonlinearities are also small. Third-order effects were evaluated by measuring the third-harmonic distortion, and the third-order two-tone intermodulation products. Shown in

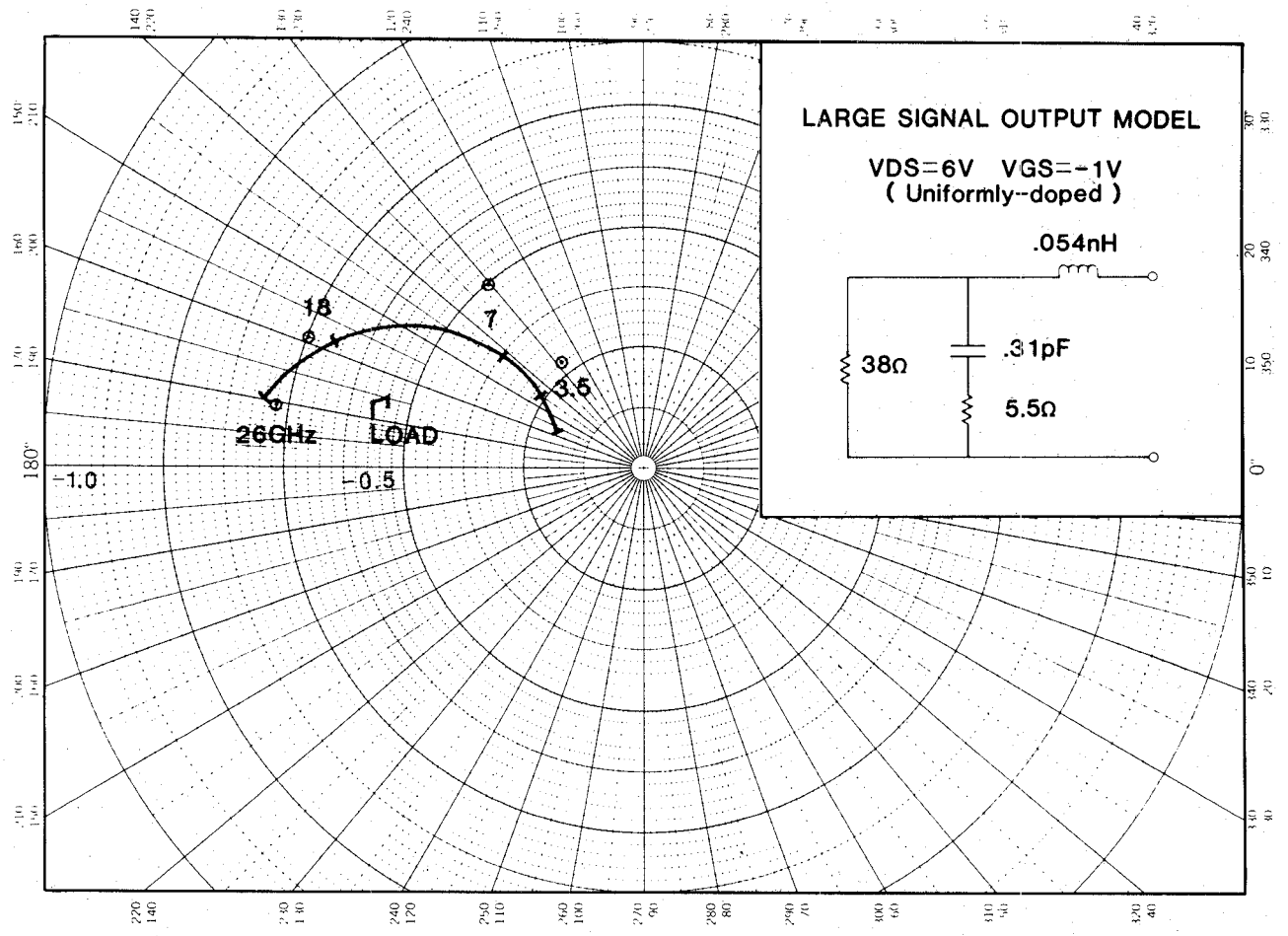


Fig. 13. Output load data for a uniformly doped FET.

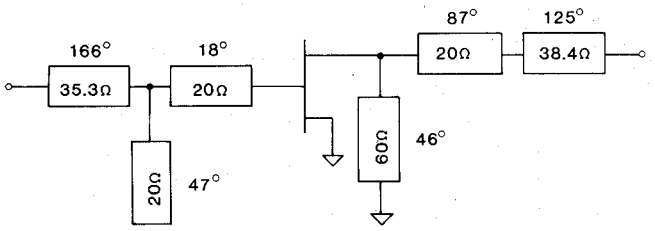


Fig. 14. A schematic diagram of the one-stage amplifier.

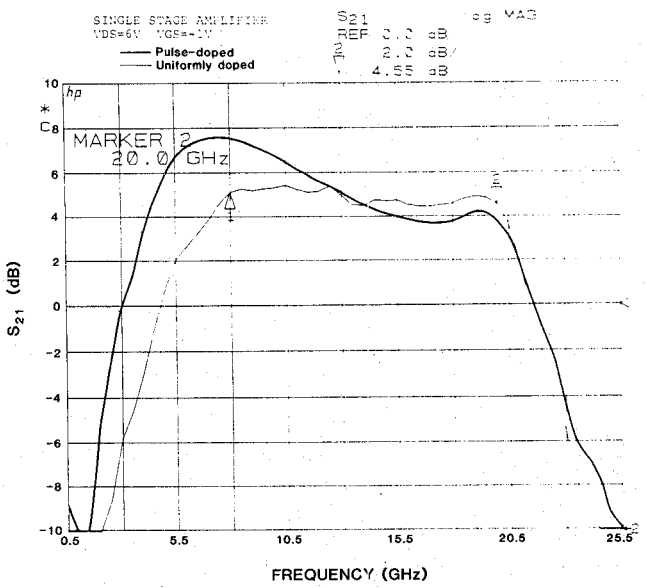


Fig. 15. Measured small-signal gain of amplifiers using (a) pulsed-doped and (b) uniformly doped FET's.

Fig. 17 is a comparison of the third-order two-tone intermodulation products for the two amplifiers. The pulse-doped FET amplifier exhibited third-order distortion products less than those of the corresponding uniformly doped FET amplifier.

VI. Summary and Conclusions

The design, fabrication, and performance of low-distortion *K*-band power FET's have been presented. The devices utilized a pulse-doped-type epi structure grown by molecular beam epitaxial techniques to achieve a very linear characteristic in transconductance versus gate voltage, which in turn reduced the harmonic distortion of the device significantly. The device features a novel 0.3 μm low-resistance T-shaped gate structure and low-inductance source backside via contacts to achieve high power and highly efficient performance up to 26 GHz. The design and performance of an 8 to 20 GHz broad-band amplifier have been presented and a 10 dBc reduction in second-harmonic

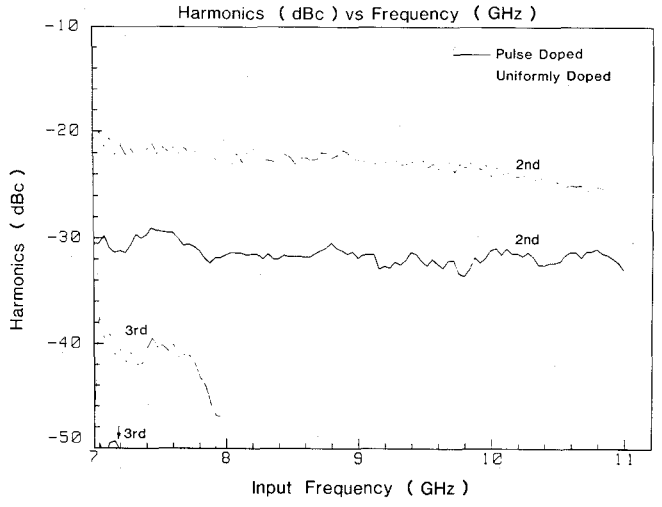


Fig. 16. Measured second- and third-harmonic distortion of the pulse-doped and uniformly doped amplifiers at 20 dBm output power.

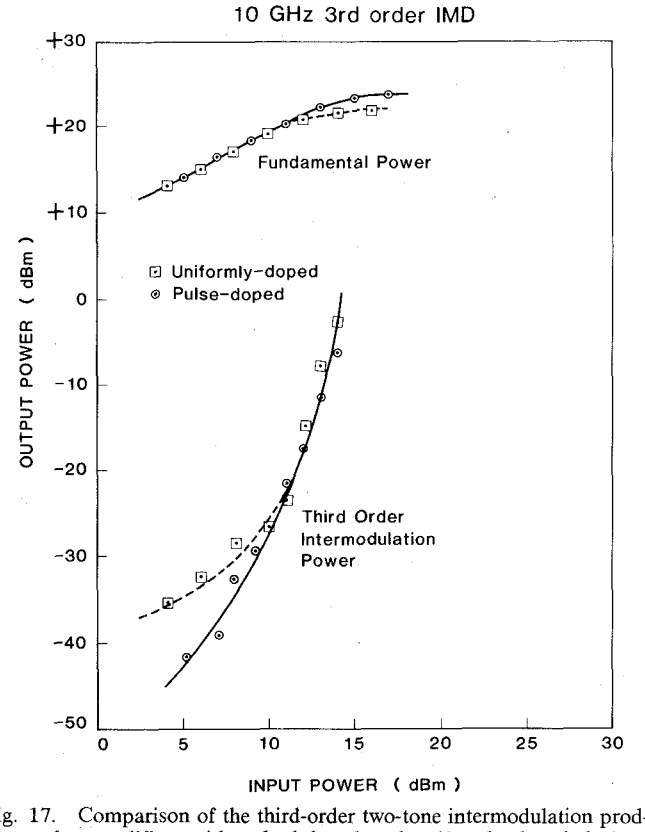


Fig. 17. Comparison of the third-order two-tone intermodulation products for amplifiers with pulsed-doped and uniformly doped devices. Signals for two-tone are two equal-amplitude signals spaced 20 MHz apart.

distortion has been achieved by using the low-distortion device as compared to a standard device fabricated on a uniformly doped epi structure.

Appendix
Derivation for Second-Harmonic Distortion Due to G_m and G_d Nonlinearities

This appendix derives expressions (1) and (2), which are the ratios of second-harmonic to fundamental due to the contribution from G_m and G_d nonlinearity, respectively.

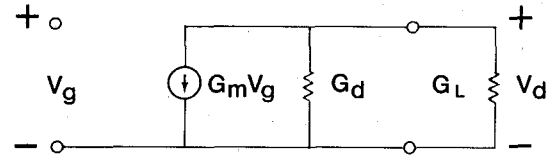


Fig. 18. Simplified equivalent circuit model for a FET.

The voltage dependence of these nonlinearities may be represented by a power series of the form

$$G_m(V_g) = G_{m0} + G_{m1}V_g + G_{m2}V_g^2 + G_{m3}V_g^3 + \cdots \quad \text{(A1)}$$

$$G_d(V_d) = G_{d0} + G_{d1}V_d + Gd_2V_d^2 + G_{d3}V_d^3 + \cdots \quad \text{(A2)}$$

where V_g and V_d represent the incremental deviations of the gate and drain voltages from the gate and drain bias voltages, respectively. Assuming a simple second-order nonlinearity, (A1) becomes

$$G_m = G_{m0} + G_{m1}V_g. \quad \text{(A3)}$$

Similarly, for a simple second-order nonlinearity (A2) becomes

$$G_d = G_{d0} + G_{d1}V_d. \quad \text{(A4)}$$

From Fig. 18,

$$V_d/V_g = -G_m/(G_d + G_L). \quad \text{(A5)}$$

For G_m nonlinearity only (i.e., $G_{d1} = 0$),

$$V_d = -\left(G_{m0}V_g + G_{m1}V_g^2\right)/(G_{d0} + G_L). \quad \text{(A6)}$$

Assuming

$$V_g = v_g \cos \omega t$$

we obtain

$$V_d = \frac{G_{m0}v_g \cos \omega t + \frac{1}{2}v_g^2 G_{m1}(1 + \cos 2\omega t)}{(G_{d0} + G_L)}. \quad \text{(A7)}$$

This yields the result

$$\text{second-harmonic/fundamental} = G_{m1}v_g/2G_{m0}. \quad \text{(A8)}$$

For G_d nonlinearity only (i.e., $G_{m1} = 0$) from (A5), we get

$$Vd = \frac{-G_{m0}V_g}{(G_{d0} + G_L)\{1 + [G_{d1}V_d/(G_{d0} + G_L)]\}}. \quad \text{(A9)}$$

Assuming

$$G_{d1}V_d/(G_{d0} + G_L) \ll 1$$

we get

$$V_d = \frac{-G_{m0}V_g}{(G_{d0} + G_L)} + \frac{G_{m0}V_gG_{d1}V_d}{(G_{d0} + G_L)^2} \quad \text{(A10)}$$

$$V_d = \frac{-G_{m0}V_g/(G_{d0} + G_L)}{1 - \left[G_{m0}V_gG_{d1}/(G_{d0} + G_L)^2\right]}. \quad \text{(A11)}$$

Assuming

$$G_{m0}V_gG_{d1}/(G_{d0}+G_L) \ll 1$$

$$V_d = \frac{-G_{m0}V_g}{(G_{d0}+G_L)}\left(1+\frac{G_{m0}V_gG_{d1}}{(G_{d0}+G_L)^2}\right). \quad \text{(A12)}$$

Substituting $V_g = v_g \cos \omega t$,

$$V_d = \frac{-G_{m0}v_g\cos\omega t}{G_{d0}+G_L} - \frac{G_{m0}^2G_{d1}v_g^2(1+\cos 2\omega t)}{2(G_{d0}+G_L)^3} \quad \text{(A13)}$$

$$\frac{\text{second-harmonic}}{\text{fundamental}} = \frac{G_{d1}G_{m0}v_g}{2(G_{d0}+G_L)^2}. \quad \text{(A14)}$$

ACKNOWLEDGMENT

The authors would like to thank J. Piercy for device fabrication, A. Cognata for device characterization, G. Patterson, M. Lightner, L. Strouse, and D. Stoughton for MBE layers, and C. Stolte for guidance and encouragement.

REFERENCES

[1] J. A. Higgins and R. L. Kuvas, "Analysis and improvement of intermodulation distortion in GaAs power FETs," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 9–17, Jan. 1980.

[2] R. E. Williams and D. W. Shaw, "Graded channel FETs: Improved linearity and noise figure," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 600–605, June 1978.

[3] R. A. Pucel, "Profile design for distortion reduction in microwave field effect transistors," *Electron. Lett.*, vol. 14, pp. 204–206, Mar. 1978.

[4] R. S. Tucker, "Third-order intermodulation distortion and gain compression in GaAs FETs," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 400–408, May 1979.

[5] P. M. White, B. Van Rees, and M. F. Leonard, "The effect of profile design, bias conditions and load impedance on intermodulation distortion in *C*-band GaAs power FETs," in *14th European Microwave Conf. Dig.*, 1984, pp. 821–826.

[6] T. S. Tan, E. Stoneham, G. Patterson, and D. Collins, "GaAs FET channel structure investigation using MBE," in *GaAs IC Symp. Tech. Dig.*, 1983, pp. 38–41.

[7] P. Bonzour *et al.*, "Saturation mechanism in 1 μm gate GaAs FET with channel-substrate interfacial barrier," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1019–1024, June 1980.

[8] K. Lehovec and R. S. Miller, "Field distribution in junction field-effect transistors at large drain voltages," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 273–281, May 1975.

[9] M. Pinto, C. S. Rafferty, and R. Dutton, "PISCES-II Poisson and continuity equation solver," Stanford Electronics Laboratory Tech. Rep., Stanford University, Sept. 1984.

[10] J. Centanni, "Two-dimensional simulation of KFET device structures using PISCES," Hewlett-Packard Co., MWTD Engineering Note no. 55, June 1987.

[11] R. Stewart, "Using PISCES to model GaAs devices," Hewlett-Packard Co., Internal Report.

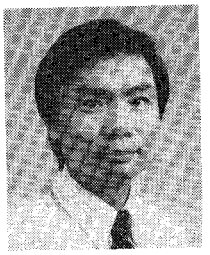
[12] S. Wemple *et al.*, "Control of gate–drain avalanche in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1013–1018, June 1980.

[13] D. Arnold, W. Kopp, R. Fischer, T. Henderson, and H. Morkoc, "Microwave performance of GaAs MESFET's with AlGaAs buffer layers—effect of heterointerfaces," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 82–84, Mar. 1984.

[14] T. S. Tan, U.S. Patent 4 618 510, Oct. 21, 1986.

[15] K. L. Kotzebue, "Microwave amplifier design with potentially unstable FET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 1–3, Jan. 1979.

[16] K. Kotzebue, T. S. Tan, and D. McQuate, "An 18 to 26.5 GHz waveguide load-pull system using active-load tuning," in *IEEE 1987 MTT-S Int. Microwave Symp. Dig.*, June 1987.



Tun S. Tan (S'70–M'77) received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1971 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1973 and 1977, respectively.

In 1976, he joined Hewlett–Packard Company, Santa Rosa, CA, and has been involved in the design, modeling, fabrication, characterization, and application of GaAs devices. He was one of the developers of the first surface-acoustic-wave resonators used in microwave instruments. He led a team of engineers for the development of *K*-band power GaAs FET's and holds a patent on a submicron gate process. He has been a development engineer, a project leader, and a project manager. His current research interests are in optoelectronic devices, photonic instruments, and coherent detection.

Dr. Tan is a member of Tau Beta Pi, Sigma Xi, and Eta Kappa Nu.

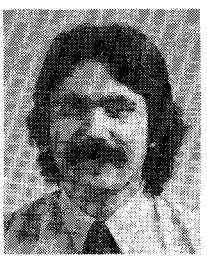
Kenneth L. Kotzebue (S'56–M'59) received the B.S. degree in mechanical engineering from the University of Texas, Austin, in 1954; the M.S. degree in engineering from UCLA in 1956; and the Ph.D. degree in electrical engineering from Stanford University in 1959.

From 1954 to 1964 he was associated with the Hughes Aircraft Company, Texas Instruments, Inc., and Watkins–Johnson Company. At Watkins–Johnson he was head of the solid-state microwave device activity and was responsible for the development of their line of magnetically tuned microwave filters. While at Watkins–Johnson he originated the YIG-tuned microwave oscillator and developed the first all-solid-state broad-band electrically tuned receiver with preselection. From 1964 to 1983 he was a member of the faculty of the Department of Electrical and Computer Engineering at UC Santa Barbara. Since 1984 he has been a part-time employee at the Hewlett–Packard Company, Santa Rosa, CA. He is the author of numerous papers and coauthor of the book *Semiconductor-Diode Parametric Amplifiers*. His current research interests are in the area of microwave monolithic integrated circuits.

David M. Braun received the B.S. and M.S. degrees in electrical engineering from the University of Wisconsin in 1978 and 1980, respectively.

In 1980, he joined the Hewlett–Packard Company, Santa Rosa, CA, as a Development Engineer. After developing processes for silicon step recovery diodes, he worked on the process design, development, and reliability of *K*-band MESFET's. Presently, he is involved with the design, development, and measurement of high-speed photodetectors.

Mr. Braun is a member of the Optical Society of America.

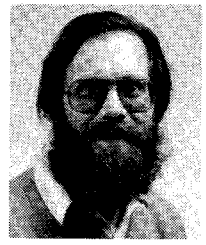


James P. Centanni received the B.A. degree in geology from San Francisco State University in 1980, and the M.A. degree in geology from the University of California, Santa Barbara, in 1984. His research thesis included the synthesis, chemical analysis, and thermal stability of a mica mineral variety.

Between 1981 and 1983 he was a teaching assistant at the University of California, Santa Barbara. In 1984, he joined the Hewlett–Packard Company, Santa Rosa, CA, and has been in-

volved with the processing, modeling, and reliability testing of GaAs power FET's.

✠



David J. McQuate received the B.S. degree (cum laude) in physics from Ohio University in 1970 and the M.S. and Ph.D. degrees in physics from the University of Colorado in 1974 and 1977, respectively.

He worked as a research assistant for the Joint Institute for Laboratory Astrophysics from 1970 to 1972, for the high energy physics group at the University of Colorado from 1972 to 1977, and for the university's liquid helium supply operation from 1977 to 1978. In 1978 he joined the Hewlett–Packard Company as a design engineer. Since then he has worked on analog, digital, and microwave circuit design for spectrum analyzers, and on the small- and large-signal characterization of GaAs FET's. He is currently involved with the design and characterization of optical components.